JOHNS HOPKINS UNIVERSITY

December 2024

PORTFOLIO REPORT

100 MS/s SAR ADC in TSMC 65 nm GP Process

High Speed Analog Design

A professional portfolio presentation of the architecture, circuit implementation, layout, and post-layout simulation performance of a high-speed, low-power SAR ADC.

100 MS/s	59.0 dB	0.685 mW	11.72 fJ
Sampling Rate	SNDR	Core Power	FOM / Step

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Acknowledgements

Thank you to Jeff Houser for his guidance, support, and technical feedback throughout this project.
His help contributed to the design review, simulation interpretation, and final presentation.

Abstract

A 100 MS/s SAR ADC implemented in the TSMC 65 nm GP process is presented. The architecture uses monotonic switching, in which the input common-mode voltage is gradually driven toward ground as the conversion proceeds. With a 1.2 V supply and a 100 MS/s sampling rate, the ADC achieves an SNDR of 59.0 dB and consumes 0.685 mW, resulting in a figure of merit of 11.72 fJ/conversion-step.

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Abbreviations

SAR	Successive Approximation Register
ADC	Analog-to-Digital Converter
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
ENOB	Effective Number of Bits
SFDR	Spurious-Free Dynamic Range
FFT	Fast Fourier Transform
FOM	Figure of Merit

CHAPTER 1

SAR Architecture

1.1 Monotonic Switching Procedure

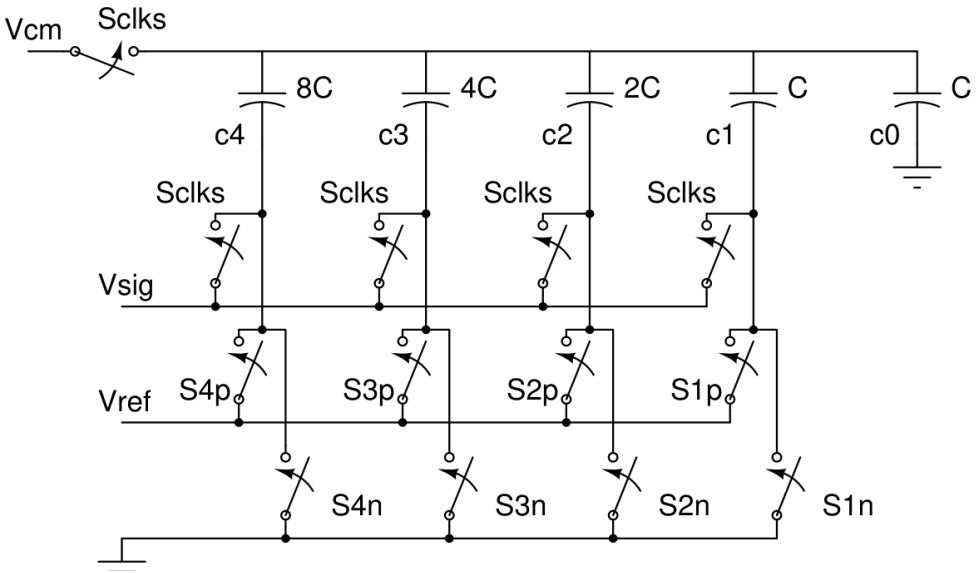

Figure 1.1: *Capacitor bank with bottom-plate sampling.*

Figure 1.1 shows a single-sided sampling capacitor bank arranged for bottom-plate sampling. A conventional SAR switching procedure for a 4-bit ADC is shown in Figure 1.2. In the conventional approach, the differential input signal is sampled onto the bottom plates of the binary-weighted capacitors. At the end of the sampling phase, the common-mode voltage connected to the top plate is turned off, and all bottom-plate voltages, except the MSB capacitor C_4, are initially set to ground. The subsequent switch sequence then evolves according to the decisions made by the comparator during successive bit resolution.

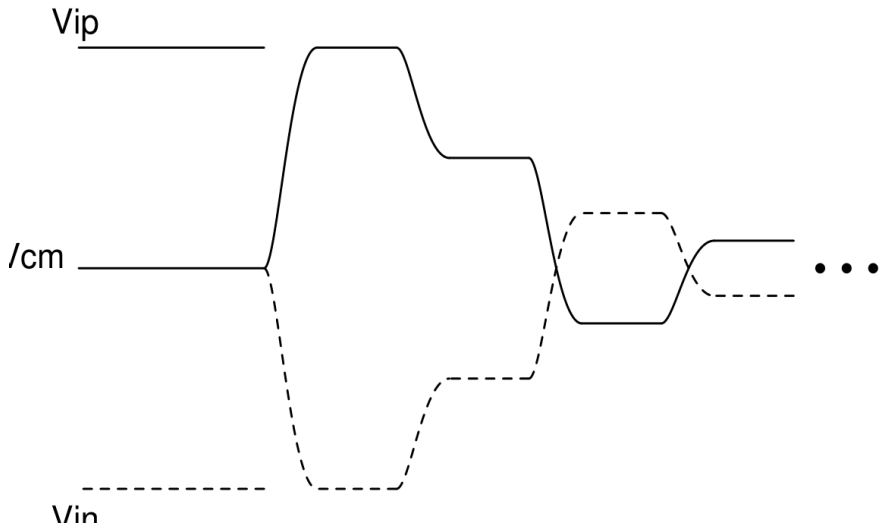

Figure 1.2: *Conventional switching procedure.*

During each conventional switching step, one capacitor bottom plate is driven to V_{ref} and then evaluated by the comparator. This method consumes unnecessary energy whenever a bottom-plate voltage must later be reset to ground. A more energy-efficient alternative is the monotonic switching procedure, where the input is sampled onto the top plate of the capacitor array rather than the bottom plate. The corresponding capacitor-bank arrangement is shown in Figure 1.3, and the monotonic switching waveform is shown in Figure 1.4.

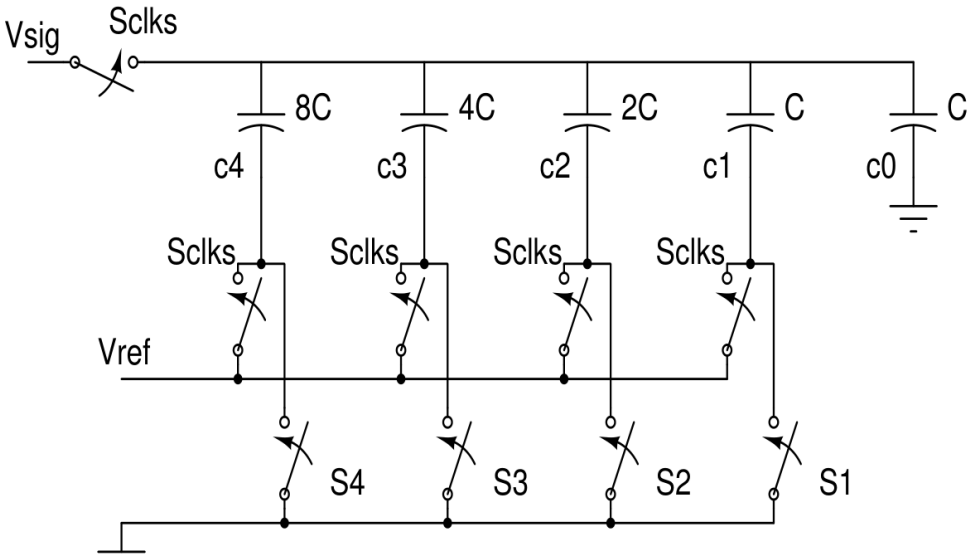

Figure 1.3: *Capacitor bank with top-plate sampling.*

With monotonic switching, a bottom plate does not need to be forced to V_{ref} before every comparison. After each decision, only one capacitor in the differential capacitor pair is switched to ground. As a result, the number of transitions remains constant regardless of input voltage. The number of monotonic transitions is also equal to the best-case number of transitions in the conventional method, excluding the mandatory initial step required by the conventional scheme.

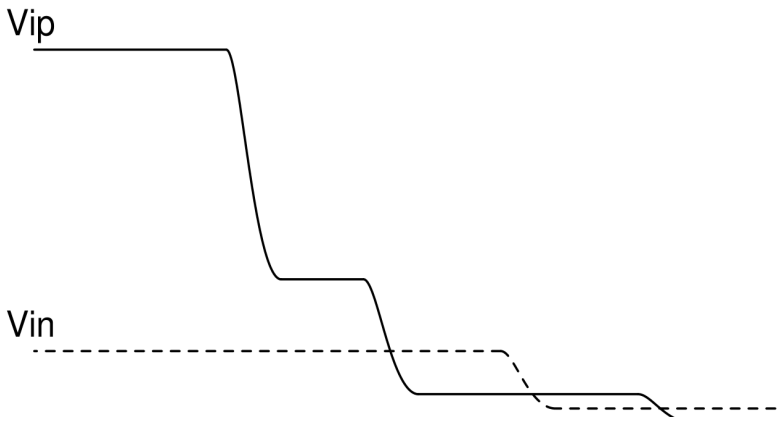

Figure 1.4: *Monotonic switching procedure.*

1.1.1 Pros and Cons of the Monotonic Switching Procedure

Pros

- The monotonic switching procedure consumes less switching power than the conventional switching method.
- Because the comparator common-mode voltage changes during each bit decision, the reference voltage and the ADC dynamic range determine the common-mode value presented at the comparator input.

- Since the input signal is sampled directly onto the top-plate capacitors, the first comparison is made directly from the sampled input. Only nine bottom-plate voltages need to be changed during the remaining bit-resolution sequence.
- Inverter-based switches are sufficient for controlling the bottom-plate voltages of the capacitors.
- The absolute voltage at the top plate of the LSB capacitor bank, which consists of capacitors 5, 4, 3, and 2, does not materially affect the top plate of the MSB capacitor bank, which consists of capacitors 10, 9, 8, 7, and 6. Therefore, the LSB top plate can be reset to V_{dd} during the sampling phase, which helps reduce the input capacitance of the SAR ADC.

Cons

- The input common-mode voltage of the differential signal at the comparator changes over the ten SAR logic cycles. This can cause the comparator input-referred offset to vary during conversion, which may degrade ADC INL and DNL.
- The drain capacitance of the bootstrapped switch and the gate capacitance of the comparator introduce gain errors. These parasitic effects limit the transistor sizes that can be used for the sampling switch and for the comparator primary differential pair.

1.2 Capacitor Bank

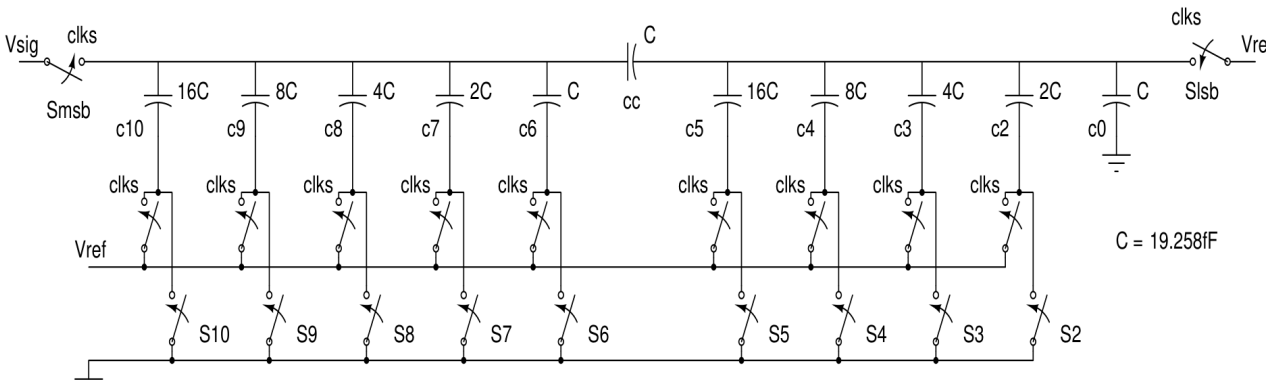

Figure 1.5: *10-bit capacitor bank used for monotonic switching.*

The schematic of the capacitor bank is shown in Figure 1.5. A conventional 10-bit binary-weighted capacitor array uses capacitor weights from 1 to 512. To reduce total capacitance, the proposed array is divided into two banks that are coupled by a capacitor with unit weight. With this split structure, the effective capacitor weights calculated at the top plate of the MSB bank, consisting of capacitors 10, 9, 8, 7, and 6, remain approximately binary.

Routing parasitic capacitance at the top plate of the LSB bank, consisting of capacitors 5, 4, 3, 2, and 0, affects the accuracy of the capacitor weights. To reduce the effect of this parasitic capacitance, capacitor C_0 is removed and the required capacitance is implemented through the routing parasitic capacitance itself. The sensitivity of the effective weights, calculated at the MSB-bank top plate, to this parasitic capacitance is relatively small. This arrangement is still more accurate than using both a physical capacitor C_0 and the unavoidable routing parasitic capacitance.

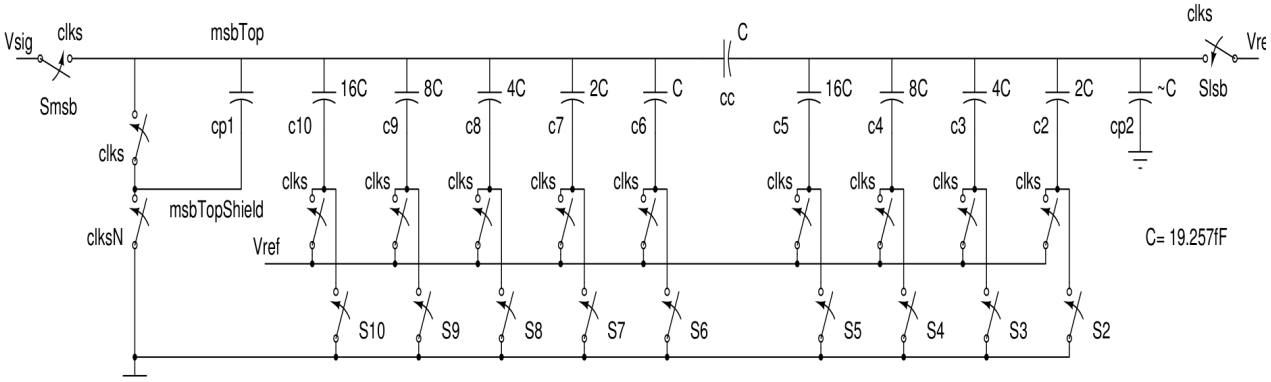

Figure 1.6: *Capacitor C_0 implemented through routing parasitic capacitance.*

In other words, the capacitor weights are more accurate when the routing parasitic capacitance is designed to approximately match the unit capacitor, instead of adding a physical capacitor C_0 in parallel with routing parasitic capacitance. Even with minimum-width routing, the parasitic capacitance cannot be reduced to a value much smaller than the unit capacitor; therefore, it is more practical to account for it directly in the capacitor-bank implementation.

As discussed in Section 1.1, parasitic capacitance at the MSB bank can introduce gain error in a monotonic switching ADC. In bottom-plate sampling, this issue is less severe because both the input signal and the DAC voltage are scaled by the same factor. Although the comparator then resolves a smaller voltage difference, that reduction can be accounted for in comparator design. A similar behavior can be emulated in the monotonic switching implementation by shielding the MSB top-plate routing.

The metal routing for the MSB top-plate node, called *msbTop*, is shielded from ground by routing another metal layer directly below it. With this shielding layer, *msbTop* has little direct parasitic capacitance to the substrate. Instead, the dominant parasitic capacitance appears between *msbTop* and the shielding node, called *msbTopShield*. During the charging phase, the shielding node is charged to the sampled signal voltage; during conversion, it is connected to ground. This method scales the input voltage by the same factor as the DAC voltages, thereby imitating the behavior of bottom-plate sampling. However, this method compensates only for routing parasitic capacitance. It does not compensate for the comparator input-gate capacitance or the sampling-switch drain capacitance.

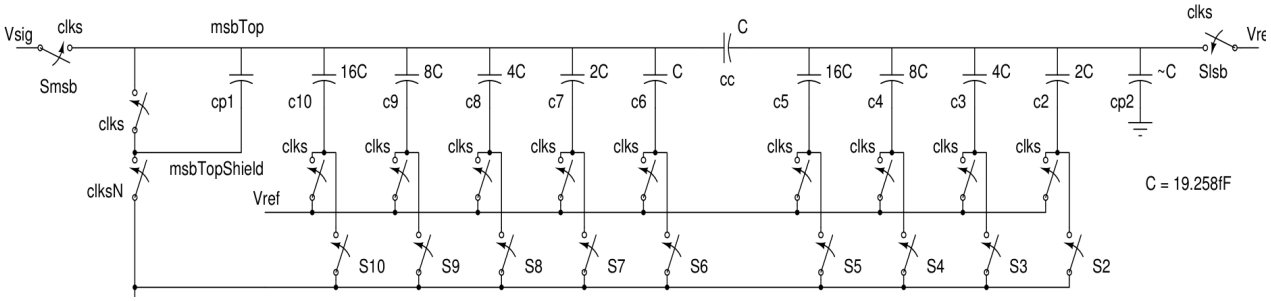

Figure 1.7: *Capacitor bank with an MSB shielding node to reduce gain error.*

Instead of connecting the shielding node directly to the signal voltage during the sampling phase, the shielding node is connected to the MSB top-plate node. This is done because the sampling switch and capacitor bank act as a filter. At high input frequencies, the signal voltage and the sampled voltage can differ slightly. Connecting *msbTopShield* to *msbTop* during sampling ensures that the shield follows the actual sampled node voltage. This shielding method is shown in Figure 1.7.

1.3 Bootstrapped Switch

The bootstrapped switch shown in Figure 1.8 is used to sample the input signal onto the top plate of the MSB capacitor bank. During the sampling phase, the LSB bank is reset to V_{ref}. The bootstrap circuit generates an approximately $V_{\text{sig}} + V_{\text{dd}}$ gate voltage for the main sampling switch M_9 during sampling, and approximately $-V_{\text{dd}}/2$ during the evaluation phase.

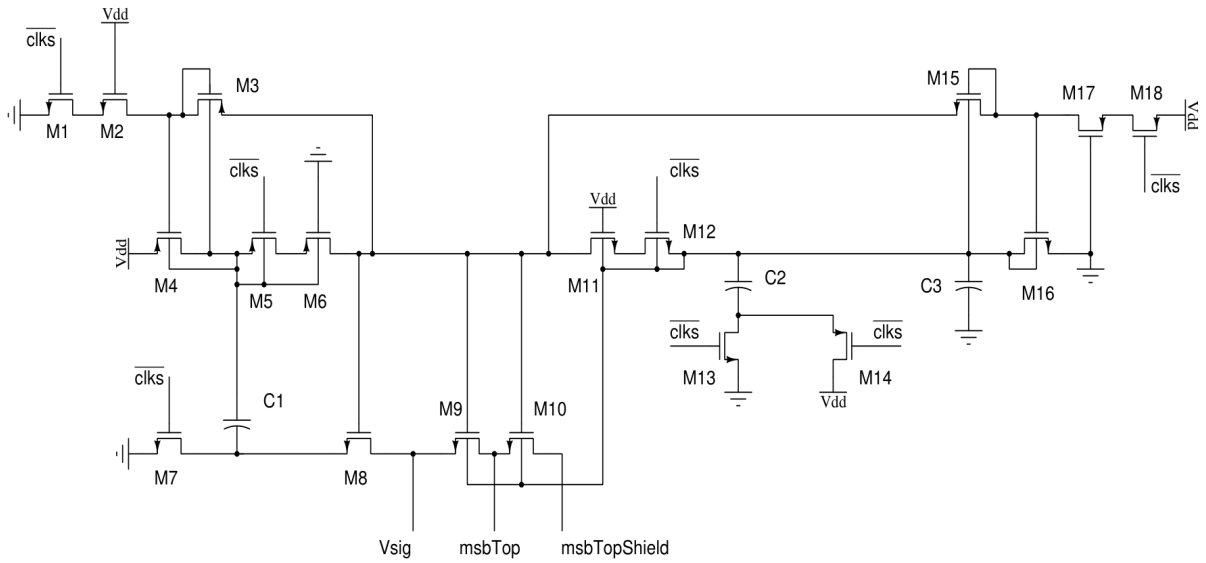

Figure 1.8: *Bootstrap switch used to sample the signal onto the capacitor bank.*

The bootstrapped switch is designed so that the voltage difference across any two transistor terminals does not exceed the nominal device voltage by a large margin. Capacitor C_1 is charged to a voltage difference of V_{dd} when *clks* is low. When *clks* goes high, the bottom plate of C_1 is connected to the input signal, and the top plate generates the required sampling-switch gate voltage, approximately $V_{\text{sig}} + V_{\text{dd}}$. This voltage is somewhat reduced by parasitic capacitance, but the strategy keeps the on-resistance of M_9 nearly constant over the input-signal range.

Capacitor C_2 generates a gate and bulk voltage of approximately $-V_{\text{dd}}/2$ while C_1 is being charged to V_{dd}. This is the phase in which the SAR ADC resolves the bits. Drain-source leakage current through M_9 can reduce ADC performance, so the gate and bulk of M_9 and M_{10} are driven to about $-V_{\text{dd}}/2$ to suppress leakage. Capacitor C_3 is adjusted after layout so that the desired $-V_{\text{dd}}/2$ voltage is generated even after including routing parasitic capacitance.

As described in Section 1.2, when *clks* is low during the ADC charging phase, *msbTopShield* is connected to the *msbTop* node. This switch is also bootstrapped and is shown as M_{10} in Figure 1.8. The separate switch that connects *msbTopShield* to ground is not shown in the figure.

Table 1.1: *Sizes of bootstrapped switch elements.*

Component	Width (μm)	Length (μm)
M1, M2, M4, M7, M8, M11, M12, M13, M14, M15, M16, M17, M18	0.24	0.06
M3, M5, M6	0.48	0.06
M9	5	0.06
M10	0.6	0.06
C1	4	4
C2	2	2

1.4 Dynamic Comparator

The schematic of the dynamic comparator is shown in Figure 1.9. This topology was selected because it provides better noise performance than a conventional strong-arm latch. As described in Section 1.1, increasing the size of the PMOS differential pair M_4 and M_5 also increases the comparator input capacitance. Because that capacitance introduces gain error, the differential-pair size cannot be increased indefinitely. To meet the noise requirements while limiting input capacitance, additional capacitors C_1 and C_2 are added at the drains of M_4 and M_5.

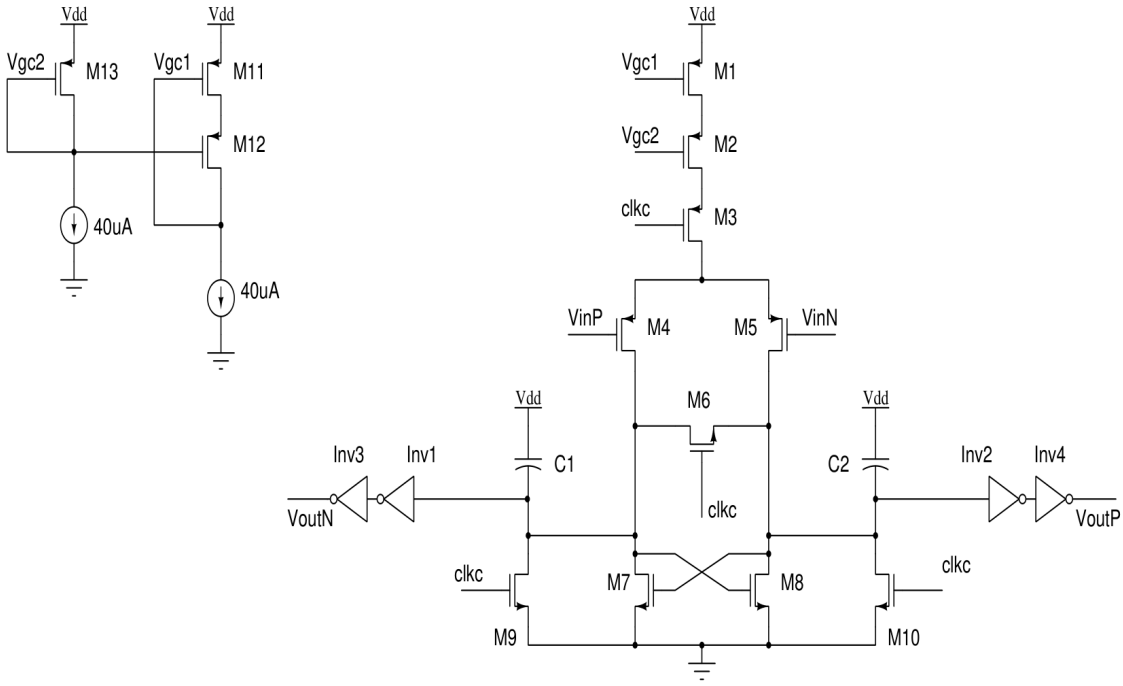

Figure 1.9: *Clocked comparator with current-source support.*

Capacitors C_1 and C_2 are implemented as NMOS capacitors connected between V_{dd} and the drain nodes. This arrangement is used because the NMOS capacitance increases as the voltage difference across it rises from 0 to V_{dd}. As a result, the capacitance variation does not oppose the regeneration process. Initially, the voltage across C_1 and C_2 is near V_{dd}, so the capacitance is at its maximum value. As the comparator regenerates the differential input, the drain voltages of M_4 and M_5 begin to rise, reducing the voltage across the capacitors. The capacitance then decreases, and the branch rising faster has lower capacitance. This reinforces, rather than slows, the regenerative decision.

The drains of M_4 and M_5 are reset to ground after each decision. Inverters 1 through 4 are added to provide rail-to-rail outputs. Although M_9 and M_{10} reset the drains of M_4 and M_5, the reset voltage of the two branches may not be identical at high speed. Transistor M_6 equalizes the two arms and ensures that both branches reset to the same voltage during the sampling phase and at the end of each conversion cycle.

The coupling caused by the drain capacitance of the sampling switch can create unequal charge injection, which introduces dynamic offset and degrades ADC performance. To reduce this effect, transistors M_1 and M_2 are used in a cascode-like arrangement to source a nearly constant average current over the comparator input common-mode range. As discussed earlier, the comparator input common-mode voltage falls from approximately $V_{\text{ref}}/2$ toward near-ground values as the SAR bits are resolved. Keeping the bias current more constant helps keep the input-referred offset more constant across common-mode voltage. A static offset in this comparator primarily creates a DC offset, but a common-mode-dependent or dynamic offset can degrade ADC performance.

When *clkc* is high, the current-source devices are not fully in saturation; however, they still ensure that the maximum possible current flows through the PMOS differential pair M_4 and M_5. Increasing the overall comparator size can also reduce dynamic offset, but it increases power consumption and reduces speed. Another offset mechanism that can degrade ADC linearity is dynamic memory offset. If the compared voltage difference is not large enough to resolve a bit cleanly, the next conversion cycle can see a comparator input voltage smaller than expected. Glitches on *clkc* can introduce this error and degrade linearity.

Table 1.2: *Comparator component sizes.*

Component	Width (μm)	Length (μm)
M1, M2	6	0.06
M3	2.4	0.06
M4, M5	1.68	0.06
M6	0.12	0.06
M7, M8	1.92	0.06
M9, M10	1.2	0.06
Inv1, Inv2	1.2	0.06
Inv3, Inv4	2.4	0.06
C1, C2	2	1

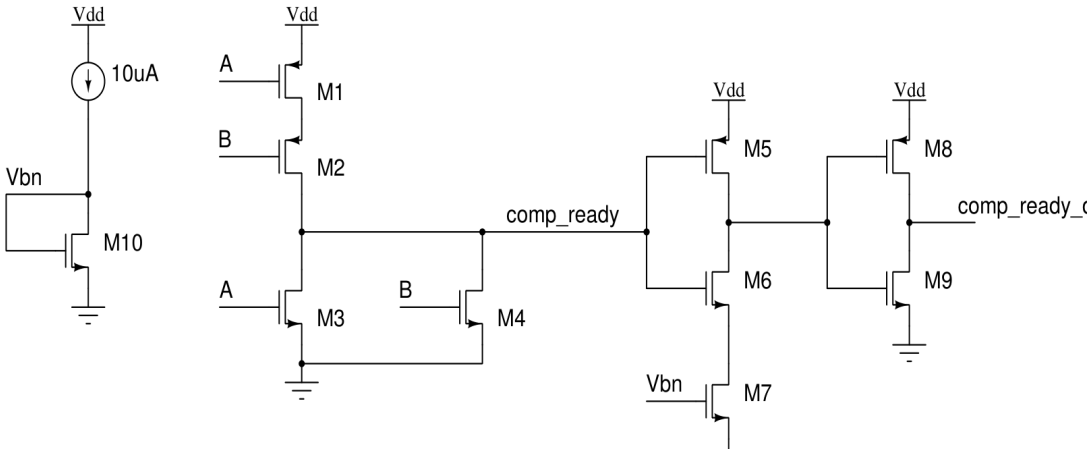

Figure 1.10: *Delay block.*

Transistors M_1 through M_4 in Figure 1.10 form a NOR gate. The comparator outputs are connected to terminals A and B, and the NOR-gate output is named *comp-ready*. When the comparator is reset, both comparator outputs

are zero. When regeneration is complete, one output becomes high while the other remains low. Therefore, the falling edge of *comp-ready* indicates that a decision has completed. The digital block uses this edge to sample and store the comparator output and then update the switch configuration.

A buffer is used to delay *comp-ready*. The buffer delay is adjusted so that the comparator is activated only after the capacitor-bank top-plate voltage has settled. As shown by the monotonic switching waveform, a finite settling time is required after each switch configuration is applied. The delay from *comp-ready* to *comp-ready-del* is the minimum practical delay at the falling edge of *comp-ready*. Unlike a conventional strong-arm latch, this comparator consumes static current after the decision is completed. Reducing the delay between the falling edge of *comp-ready* and the next rising edge of *clkc* therefore helps reduce comparator power consumption.

1.5 SAR Control Logic

An asynchronous control circuit is used inside the ADC to generate the required clock signals for the switching circuitry. The conventional digital logic is shown in Figure 1.11. In that structure, the delay from *comp-ready* to $sw(n)$ is dominated by two flip-flop delays: the delay from *comp-ready* to $clk(n)$ and the delay from $clk(n)$ to $sw(n)$. At high conversion speeds, accommodating two flip-flop delays in the critical loop is difficult.

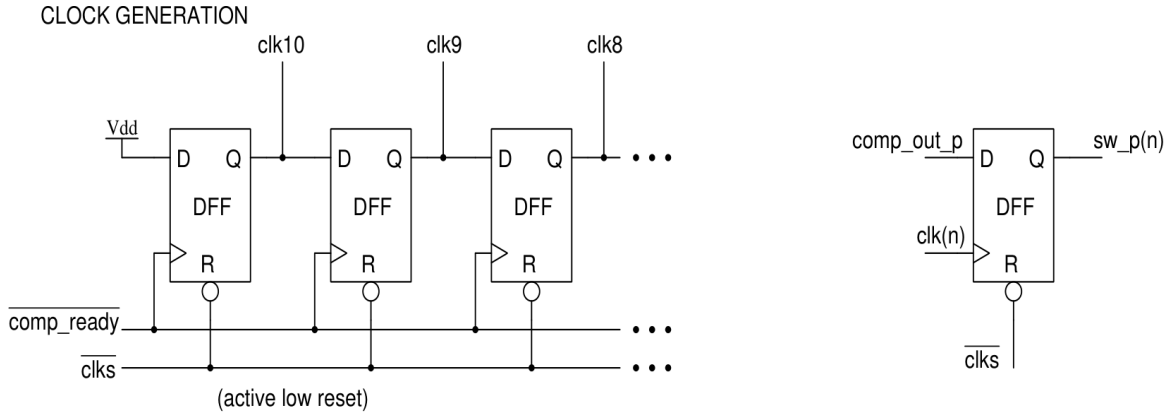

Figure 1.11: *Conventional SAR logic.*

To reduce the critical timing delay, a modified arrangement is used as shown in Figure 1.12. Rather than generating the required clock on the falling edge of *comp-ready*, when timing is most critical, the required clock-enable signals are generated on the rising edge of *comp-ready*. When the falling edge of *comp-ready* arrives, the delay from *comp-ready* to $clk(n)$ is caused only by a NOR gate. The total delay from *comp-ready* to $sw(n)$ is therefore reduced to one NOR-gate delay plus one flip-flop delay.

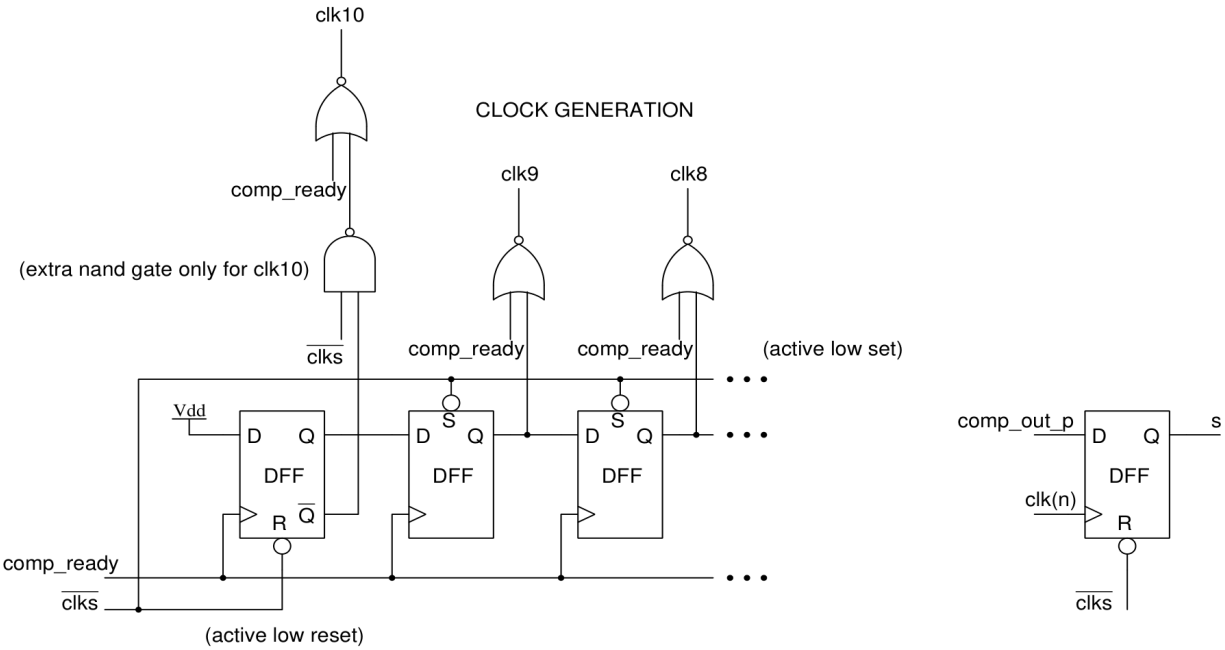

Figure 1.12: *Proposed SAR logic.*

Because flip-flop delays are significantly larger than combinational-logic delays, the proposed arrangement in Figure 1.12 reduces delay compared with the conventional arrangement in Figure 1.11. An additional NAND gate is inserted only in the *comp-ready* to $clk10$ path to ensure that $clk10$ is activated only after *clks* goes low. Since the total number of gates is small, leakage power is not a significant concern. Foundry standard cells were used for the layout of the control-logic block.

The timing diagram of the generated clocks is shown in Figure 1.13. Clocks $clk1$ through $clk10$ sample the digital output codes of the comparator and also serve as switch-control signals for the capacitor bank during the monotonic switching procedure.

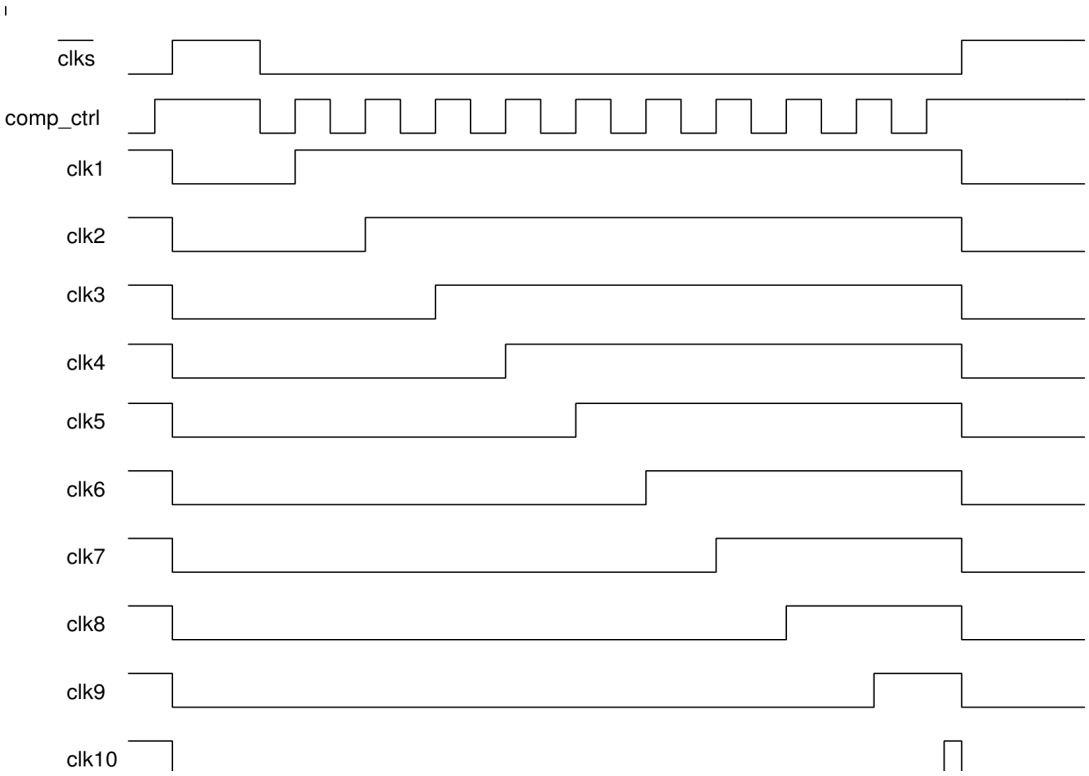

Figure 1.13: *Timing diagram of the control logic.*

CHAPTER 2

Layout and Simulation Results

The SAR ADC was laid out in the TSMC 65 nm technology using the Cadence Virtuoso tool. The area occupied by the SAR ADC core is 276 μm $\times$ 135 μm. Layouts of the main circuit blocks are shown below.

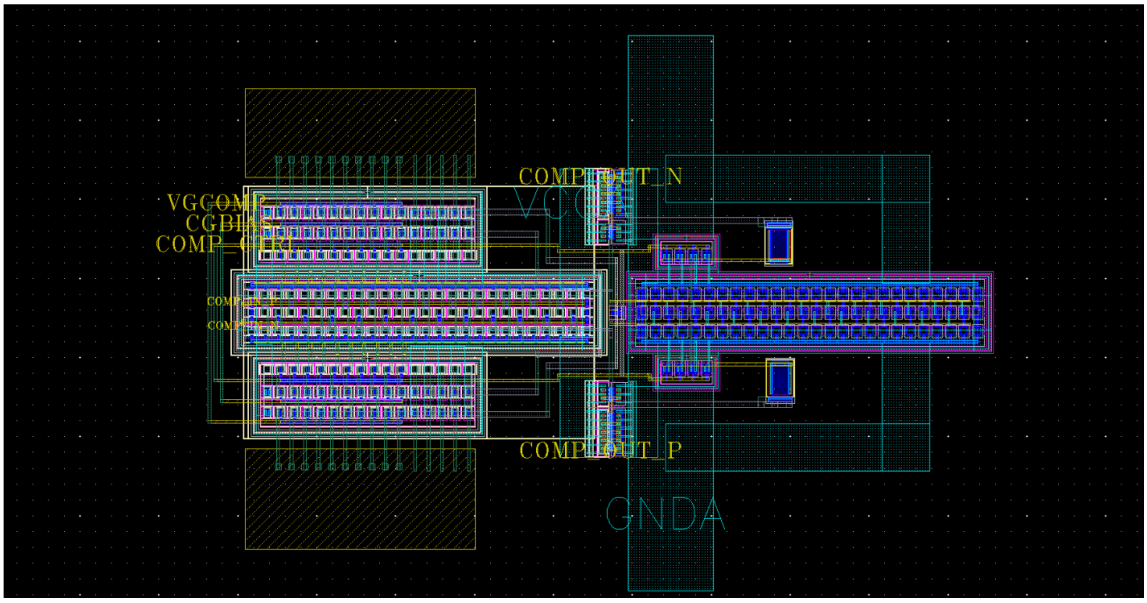

Figure 2.1: *Layout of the comparator.*

The input pair and regenerative transistors are laid out using an interdigitized technique to reduce mismatch.

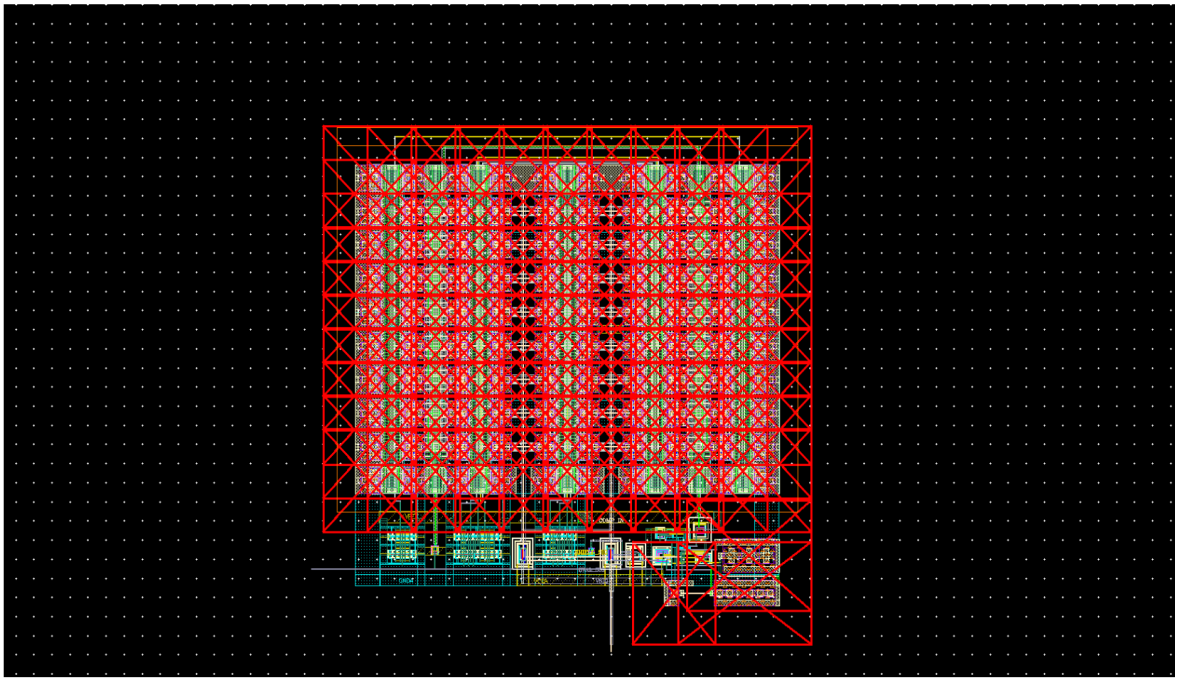

Figure 2.2: *Layout of the capacitor bank with the bootstrapped switch.*

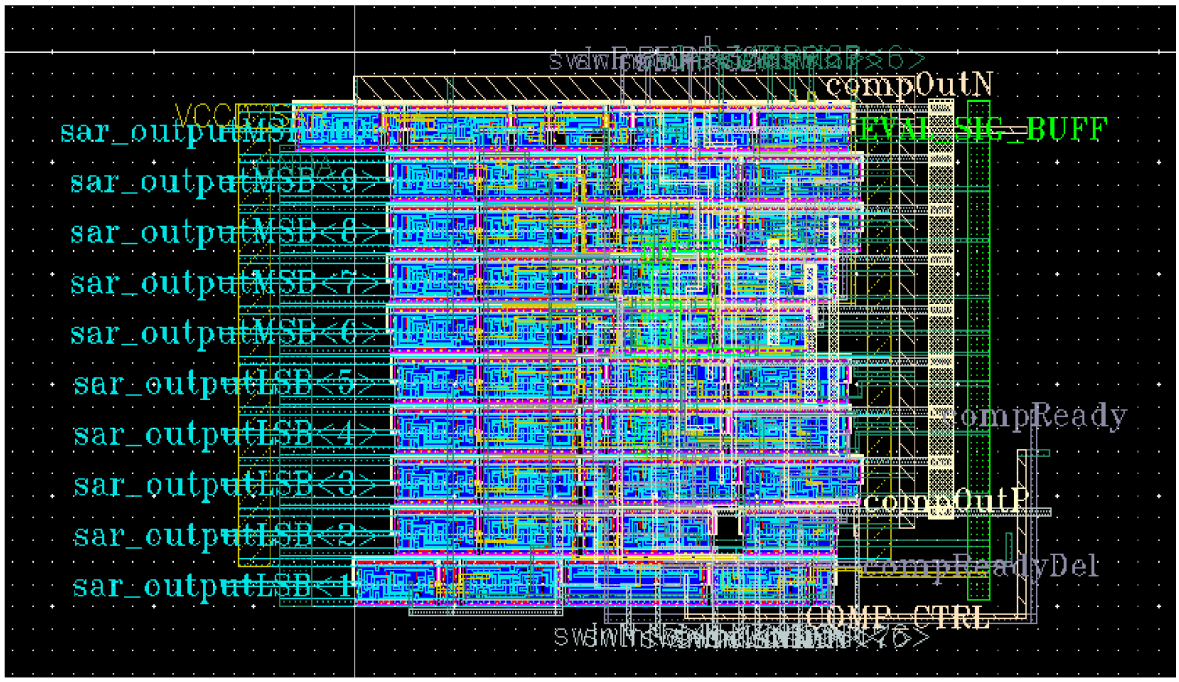

Figure 2.3: *Layout of the SAR control logic.*

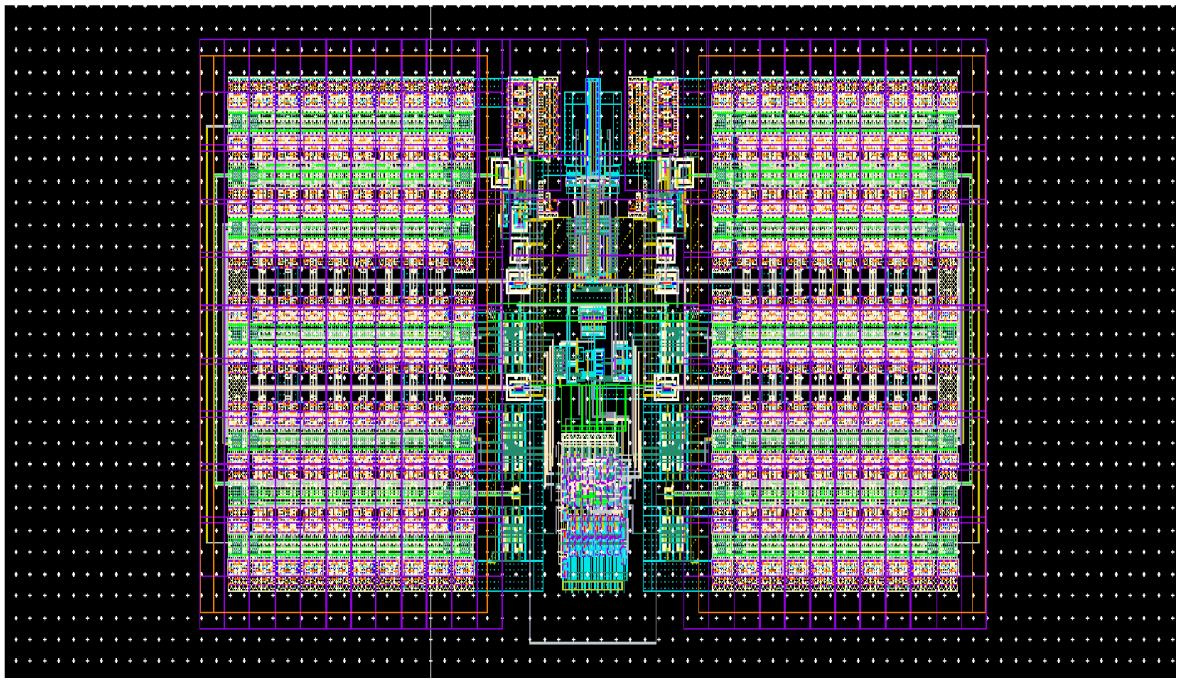

Figure 2.4: *Layout of the SAR ADC core.*

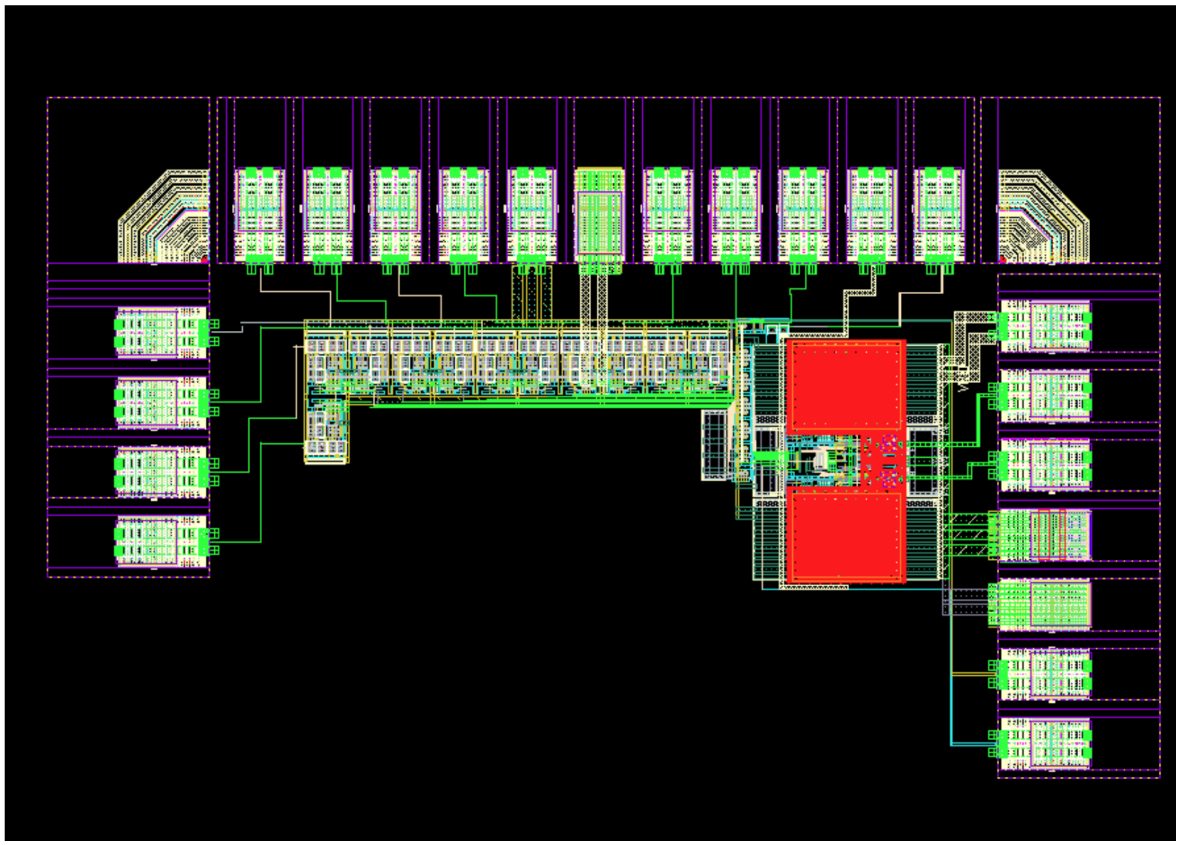

Figure 2.5: *Full chip layout with I/O pads.*

2.1 Simulation Results

The nominal supply voltage is 1.2 V. The input applied for full-scale output has a 580 mV amplitude, corresponding to a 1160 $mV_{pk\text{-}pk}$ differential amplitude.

2.1.1 Inverter Switches

The unit inverter devices are sized as follows:

- PMOS: 480 nm / 60 nm
- NMOS: 720 nm / 60 nm, using an LVT device

These inverter units are scaled appropriately to implement the capacitor-bank switches. The worst-case settling time is observed at the SS process corner. Using the equivalent $10RC$ settling time, the worst-case settling time is 54.5 ps.

2.1.2 Capacitor Bank

The unit capacitance is a 19.258 ± 16.5% fF MIM capacitor. The $\sqrt{kT/C}$ noise at 300 K is 89.18 μV.

2.1.3 Comparator

Comparator noise was simulated using the PSS/Pnoise method, which provides a more efficient noise estimate than extensive transient-noise simulation. The Cadence noise summary showed that flicker noise from the

input differential pair and the regenerative pair were the main noise contributors. A 500-sample Monte Carlo simulation was also run to estimate the dynamic-comparator offset. The resulting comparator performance is summarized in Table 2.1.

Table 2.1: *Comparator noise and mismatch performance.*

Parameter	Value
Input-referred noise (rms)	700 μV
Input-referred offset due to mismatch	9.71 mV

2.1.4 SAR ADC Dynamic Performance

The fully assembled SAR ADC was simulated with an R+C+CC parasitic-extracted netlist. The input was a single-ended sinusoid with 580 mV amplitude and a 600 mV common-mode voltage. The ADC was simulated across the process corners summarized in Tables 2.2 and 2.3. The power consumption of the main core blocks is shown in Table 2.4. A 256-point FFT digital output spectrum simulated at the TT corner is shown in Figure 2.6.

Table 2.2: *ADC dynamic performance at* $\frac{13}{128} \times 100$ *MHz input frequency.*

Parameter	SF	SS	FF	FS	TT
ENOB (bits)	9.49	9.58	9.35	9.512	9.51
SINAD (dB)	58.91	59.45	58.04	59.03	59.02
SFDR (dBc)	66.81	67.96	66.10	65.13	66.59

Table 2.3: *ADC dynamic performance at* $\frac{61}{128} \times 100$ *MHz input frequency.*

Parameter	SF	SS	FF	FS	TT
ENOB (bits)	9.31	9.38	9.27	9.40	9.26
SINAD (dB)	57.85	58.22	57.60	58.38	57.52
SFDR (dBc)	63.67	63.23	62.50	64.75	63.83

Table 2.4: *Power consumed by the main core blocks.*

Block	Power Consumption (μW)
Comparator	210
Capacitor Bank	30
Delay Block + Core Buffers	200
SAR Control Logic	245
Total	685

The figure of merit is calculated using

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min\left[f_s, 2 \times \text{ERBW}\right]}. \tag{2.1}$$

For the extracted ADC simulation,

$$\text{FOM} = \frac{685 \times 10^{-6}}{2^{9.26} \times 100 \times 10^{6}} = 11.72 \text{ fJ/conversion-step.} \tag{2.2}$$

A transient-noise analysis was run for four cycles of 256 points. The mean values of the measured parameters were used to represent the dynamic performance with random noise generated by the ADC. The measured dynamic performance with transient noise is:

- ENOB = 9.336 bits
- SINAD = 57.96 dB
- SFDR = 67.24 dBc

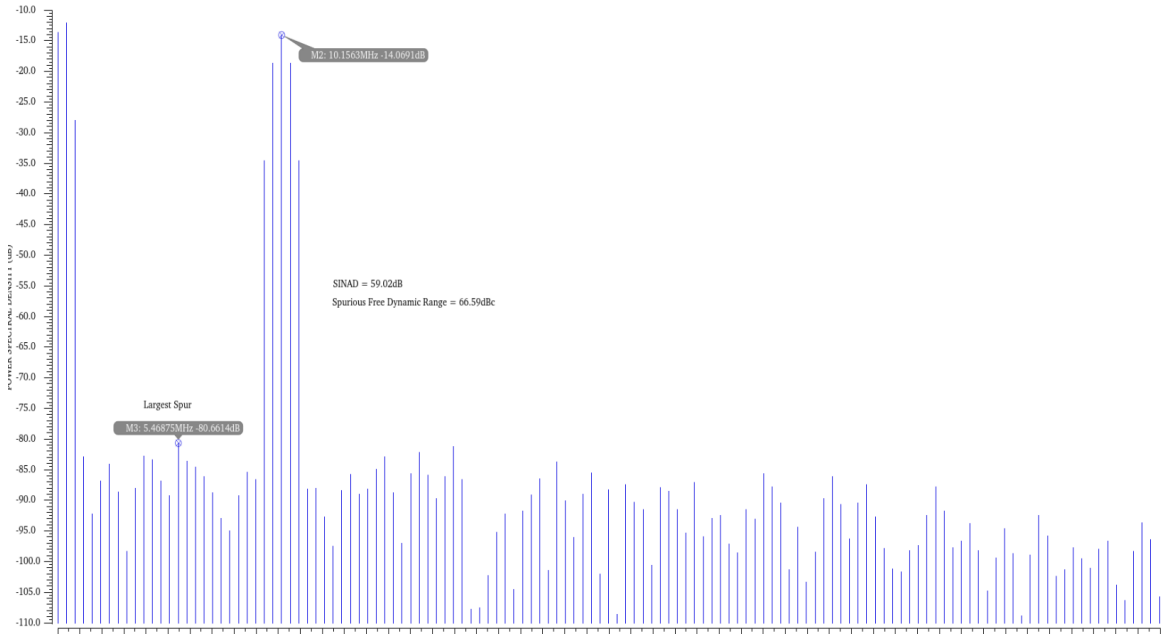

Figure 2.6: *256-point FFT digital output spectrum across the TT corner.*